ABSTRACT

In a nonrecursive digital filter, the number of times each bit of input data passes through a shift register is reduced to save power.

Despreading data is sent to a first shift register 21 and a second shift register 22 each having a number of stages obtained by dividing the usual number of stages by two, and both shift registers alternately perform a shift operation at both edges of a shift clock CK. Multiplexers MP11 to MP14 are provided for selecting the odd-numbered codes of reference codes stored in a reference-code register 23 when the shift clock CK is in an OFF state and for selecting the even-numbered codes when the shift clock CK is in an ON state, and multiplexers MP21 to MP24 are provided for performing the selections analogous to the above. The exclusive-OR output of the output of each stage of the first shift register 21 and the outputs of the multiplexers MP11 to MP14, and the exclusive-OR output of the output of each stage of the second shift register 22 and the outputs of the multiplexers MP21 to MP24 are added by the adder 25 to obtain a correlation-strength output.